Electronic Version
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Claims

[c1] What is claimed is:

1.A partially depleted SOI MOS device comprising:

a well of first conductivity type isolated in a thin film body of an SOI substrate, said SOI substrate comprising said thin film body, a support substrate and a buried oxide layer interposed between said thin film body and said support substrate;

a gate dielectric layer on a surface of said well;

a polysilicon gate on said gate dielectric layer, said polysilicon gate consisting of a first gate section of first conductivity type overlapping with an extended well region of said well and a second gate section of second conductivity type lying across said well, whereby a tunneling connection is formed between said first gate section and said extended well region of said well; and

source and drain regions of second conductivity type on opposite sides of said second gate section.

[c2] 2.The partially depleted SOI MOS device according to claim 1 wherein said gate dielectric layer is selected from the group consisting of silicon dioxide, nitrogen contained silicon dioxide, oxynitride, and Al, Zr, La, Ta, or

Hf contained high K dielectric layer.

[c3] 3.The partially depleted SOI MOS device according to claim 1 wherein said dielectric layer has a thickness of between about 5~120 angstroms.

[c4] 4.The partially depleted SOI MOS device according to claim 1 wherein said thin film body is a silicon layer.

[c5] 5.The partially depleted SOI MOS device according to claim 1 wherein said first conductivity type is N type, and said second conductivity type is P type.

[c6] 6.The partially depleted SOI MOS device according to claim 1 wherein said first conductivity type is P type, and said second conductivity type is N type.

[c7] 7.A partially depleted SOI MOS device comprising:
a silicon wafer having a thin film body, a supporting substrate, and a buried oxide layer isolating said thin film body from said supporting substrate, said thin film body having a main surface;
oxide filled trenches that extend downwards from said main surface as far as said buried layer, said trenches being disposed so as to fully enclose a volume of said thin film body, thereby forming a well on said main surface;
a gate dielectric layer on said main surface;

a polysilicon gate of first conductivity type on said gate dielectric layer, said polysilicon gate having two opposing long sides that extend from a first end over a first oxide filled trench across said well to a second end over a second oxide filled trench, wherein a portion of one of said ends of said polysilicon gate is implanted with ions of second conductivity type opposite to said first conductivity type, whereby a tunneling connection is formed between said well and said implanted portion of said polysilicon gate; and

source and drain regions of first conductivity type on opposite sides of said polysilicon gate.

[c8] 8.The partially depleted SOI MOS device according to claim 7 wherein said dielectric layer is selected from the group consisting of silicon dioxide, nitrogen contained silicon dioxide, oxynitride, and Al, Zr, La, Ta, or Hf contained high K dielectric layer.

[c9] 9.The partially depleted SOI MOS device according to claim 7 wherein said dielectric layer has a thickness of between about 5~120 angstroms.

[c10] 10.The partially depleted SOI MOS device according to claim 7 wherein said thin film body is a silicon layer.

[c11] 11.The partially depleted SOI MOS device according to

claim 7 wherein said first conductivity type is P type, and said second conductivity type is N type.

[c12] 12.The partially depleted SOI MOS device according to claim 7 wherein said first conductivity type is N type, and said second conductivity type is P type.